WE CLAIM:

1. a replica Gm cell comprising:

at least one Gm setting device;

a pair of input transistors connected with said Gm setting device, each input transistor operable to receive a reference voltage;

an error amplifier connected with said pair of input transistors;

a reference current source connected with said error amplifier; and

a current mirror connected with said error amplifier.

2. The replica Gm cell of Claim 1 wherein said at least one Gm setting device comprises a pair of transistors, said transistors having gates that are tied together.

3. The replica Gm cell of Claim 1 wherein said at least one Gm setting device comprises a plurality of transistors, said transistors having sources that are tied together and drains that are tied together.

4. The replica Gm cell of Claim 1 wherein said at least one Gm setting device is arranged in a binary coded configuration.

5. The replica Gm cell of Claim 1 wherein said at least one Gm setting device is arranged in a thermometer coding configuration.

6. The replica Gm cell of Claim 1 wherein said at least one Gm setting device is arranged in a segmented thermometer coding configuration.

7. The replica Gm cell of Claim 1 wherein each of said input transistors are operable to receive a reference voltage.

~~9.~~ 8 The replica Gm cell of Claim 1 wherein said reference current source comprises a current multiplying digital-to-analog converter.

~~10.~~ 9 The replica Gm cell of Claim 1 wherein said reference current source comprises a current multiplying digital to analog converter and a current mirror.

~~11.~~ 10 The replica Gm cell of Claim 1 further comprising a tail current source connected with said reference current source.

~~12.~~ 11 The replica Gm cell of Claim 1 wherein said current mirror comprises:

a mirror reference transistor, said mirror reference transistor having a gate, source, and drain connected with a first input of said error amplifier; and

a mirrored pull-up current source, said mirrored pull-up current source having a gate connected with said gate of said mirror reference transistor and said first input of said error amplifier, a source connected with said source of said mirror reference transistor, and a drain connected with a second input of said error amplifier.

~~13.~~ 12 The replica Gm cell of Claim 1 wherein said current mirror comprises:

a mirror reference transistor, said mirror reference transistor having a gate, a source, and a drain;

a first cascode transistor, said first cascode transistor having a gate, a source connected with the drain of said mirror reference transistor, and a drain connected with a first input of said error amplifier;

a mirrored pull-up current source, said mirrored pull-up current source having a gate connected with said gate of said mirror reference transistor and said first input of said error amplifier, a source connected with said source of said mirror reference transistor, and a drain;

a second cascode transistor, said second cascode transistor having a gate connected with said gate of said first cascode transistor, a source connected with the drain of said mirrored pull-up current source, and a drain connected with a second input of said error amplifier.

~~14.~~ 13 a replica Gm cell comprising:

a digital to analog converter, said digital to analog converter operable to receive a Gm setting code and output a current having a magnitude proportional to said Gm setting code;

a current mirror connected with said digital-to-analog converter;

a mirror reference transistor connected with said current mirror;

a mirrored pull-up current source connected with said current mirror and said mirror reference transistor;

a tail current source connected with said digital to analog converter;

at least one Gm setting device connected with said tail current source;

a first input transistor connected with said at least one Gm setting device;

a second input transistor connected with said at least one Gm setting device; and

an error amplifier operable to provide a tuning voltage to said Gm setting device, said error amplifier having a first input and a second input,

wherein said error amplifier generates said tuning voltage by comparing a first voltage located between said first input transistor and said mirrored pull-up current source with a second voltage located between said second input transistor and said mirror reference transistor.

~~15~~ 14. The replica Gm cell of Claim ~~14~~ 13 further comprising a first cascode transistor connected with said mirrored pull-up current source and said first input of said error amplifier and second cascode transistor connected with said mirror reference transistor and said second input of said error amplifier.

~~16~~ 15. The replica Gm cell of Claim ~~14~~ 13 further comprising a first cascode transistor connected with said first input transistor and said error amplifier and a second cascode transistor connected with said second input transistor and said error amplifier.

~~17~~ 16. The replica Gm cell of Claim ~~14~~ 13 wherein said at least one Gm setting device comprises a plurality of Gm setting devices, each of said Gm setting devices comprising at least one transistor with a source, gate, and drain and said plurality of Gm setting devices having said sources tied together and said drains tied together.

18. The replica Gm cell of Claim 17 further comprising a switching circuit connected with said plurality of Gm setting devices and operable to receive said Gm setting code and provide a voltage to said gates of said Gm setting devices.

19. The replica Gm cell of Claim 17 wherein said digital to analog converter is operable to receive a Gm setting code having a number of bits greater than a number of Gm setting devices.

20. A method for calibrating a Gm cell comprising the acts of:

providing a Gm cell;

providing a replica Gm cell connected with said Gm cell;

providing a high reference voltage and a low reference voltage to said Gm cell;

providing a Gm setting code to said Gm replica cell;

generating a tuning voltage utilizing said replica Gm cell;

adjusting said tuning voltage until the difference between a pair of drain currents that flow through a pair of input transistors is substantially equal to a reference current;

utilizing the tuning voltage generated by said replica Gm cell in said Gm cell.

21. The method of claim 20, further comprising the act of providing said Gm setting code to said Gm cell.

22. The method of claim 20, further comprising the act of generating a bias voltage to said Gm cell utilizing to said Gm replica cell.

23. A digitally programmable generalized biquad comprising:

a first Gm cell operable to receive a differential voltage input and a tuning voltage and generate a differential voltage output;

a second Gm cell operable to receive a differential voltage input and a tuning voltage and generate a differential voltage output;

a first replica Gm cell operable to receive a high reference voltage, a low reference voltage, and a Gm setting code and generate a tuning voltage, said first replica Gm cell connected with said first Gm cell;

a second replica Gm cell operable to receive a high reference voltage, a low reference voltage, and a Gm setting code and generate a tuning voltage, said second replica Gm cell connected with said second Gm cell;

a first common mode feedback circuit connected with said first Gm cell; and

a second common mode feedback circuit connected with said second Gm cell.

24. 23 The digitally programmable generalized biquad of claim ~~23~~ 22 wherein said first Gm cell and said second Gm cell are operable to receive said Gm setting code.

~~25~~ 24. The digitally programmable generalized biquad of claim ~~23~~ 22 wherein said first replica Gm cell is operable to generate a bias voltage and said first Gm cell is operable to receive said bias voltage.

~~26~~ 25 The digitally programmable generalized biquad of claim ~~23~~ 22 wherein said second replica Gm cell is operable to generate a bias voltage and said second Gm cell is operable to receive said bias voltage.

~~27~~ 26 The digitally programmable generalized biquad of claim ~~23~~ 22 further comprising at least one additional first Gm cell connected with said first Gm replica cell.